IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:		)		
Shivnandan D Kaushik et al. for **Intel Corporation**		))		
Serial No.:	10/028,858	)	Group Art Unit:	2112
Filed:	December 19, 2001	)	Examiner:	Zaman, Faisal M.

FOR: **HOT PLUG INTERFACE CONTROL METHOD AND APPARATUS**

REPLY BRIEF IN SUPPORT OF APPELLANT'S APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

Appellants hereby reply to the Examiner's Answer dated December 6, 2006.

Filed EFS–Web on February 6, 2007

Claims 1-5, 7-10, 28, 29, 35 and 37 are the subject of the appeal. The Examiner has maintained rejection of the claims 1-5, 7-10, 28, 29, 35 and 37.

Claims 1-10, and 16-38 are pending. Claims 16-27 and 31-34 have been allowed. Claims 1-5, 7-10, 28, 29, 35 and 37 have been rejected. Claims 6, 30, 36 and 38 have been objected to and would be allowable if rewritten in independent form to include each and every limitation of the base claim and any intervening claim. Claims 11-15 have been cancelled.

All of the arguments in Appellant's Appeal Brief ("Appeal Brief"), filed on October 2, 2006, are herein incorporated into this Reply Brief to the Examiner's Answer.

Before responding to the arguments provided in the Examiner's Answer, it is respectfully submitted that several technical aspects of the Examiner's Answer remain inaccurate and problematic.

The Examiner has presumed that processor cards 11, 20 and 30 in Bealkowski et al. ("Bealkowski") (U.S. Patent No. 6,282,596) have communication interfaces, which are enabled when hot plugged to a computing system. Appellants respectfully submitted in the First Appeal Brief dated July 6, 2005 and again in the reply filed on November 28, 2005 that the items 11, 20 and 30 appears to have power interface which do not appear to be similar to the communication interface on the hot plug as required by the Appellant's claims.

Appellants respectfully submit that items 11a-d, 20a-d and 30a-d are processor cards, voltage regulator modules (VRM) and processors (CPU), respectively, as named

in Bealkowski. A processor card 11 comprises the CPU and the VRM (see column 2, lines 22-27 and lines 37-42 of Bealkowski). The processor cards 11 may have power interfaces, but do not appear to establish communication link to transfer data, when it is hot plugged.

In addition, the Examiner has presumed that slot connector 16, disclosed by Olarig et al. ("Olarig")(U.S. Patent No. 6,587,909) has a communication interface to establish a communication link with a computing system in order to transfer data. Applicants have respectfully and repeatedly submitted that the slot connector is used to provide power to turn on the circuitry on the memory module and does not appear to have a communication interface. Appellants submit that the slot connector should have a built-in intelligence to establish the communication link. Olarig does not teach that the slot connector is capable to establish the communication link with the computing system in order to transfer data.

Appellants now address the merit of the new arguments put forth, by the Examiner in the Examiner's Answer to the Appellant's Appeal Brief, with regard to the rejected claims.

The Examiner rejected **claims 1, 7, 8 and 9** under 35 USC 102(e) as being anticipated by Olarig. Appellants respectfully submit that each of claims 1 and 7, 8 and 9 requires ***enabling a communication interface on a hot plug module to establish a communication link with a running computing device***. In the newly cited column 6, lines 50-57, Olarig discloses that the memory controller 12 first provides power to the

slot connector 16 by connecting the power lines to the slot connector. After allowing the power on the memory module inserted in the slot connector 16 to stabilize, the memory controller 12 then connects the clock line to the slot connector 16. Because the clock line is connected to the slot connector 16 after the power lines, circuitry on the memory module is fully turned on before the circuitry is driven by a clock signal.

However, Olarig does not appear to teach the ***communication interface on a hot plug module and how it is enabled to establish the communication link*** as required by claims 1, 7, 8 and 9. In contrast to the claimed invention, Olarig discloses a power up sequence for slot connector that holds an SDRAM memory module and turning on the memory module before the circuitry is driven by a clock signal.

Further, the Examiner's Answer states, "In the context of the Olarig reference, the "enabling" function can be equated to the computer system 10 sending a signal to activate power within memory modules 14 as they are inserted into slot 16. Appellants submit that Olarig teaches to send a signal to activate power within the memory module. However, data transfer can not take place unless a communication interface meant for the transfer of data is enabled. Appellants submit that a person skilled in the art would not interpret, "sending a signal to activate power within memory module" to be similar to "enabling a ***communication interface on a hot plug module*** to establish a ***communication link*** with a running computing device". Appellants submit that in addition to a power interface, a communication interface on the hot plug module may be required to establish communication link with the running computing device in order to

perform required functions (Please see FIG. 1 and paragraphs 17, 18 and 19 of the present application).

Thus, Olarig does not teach enabling a ***communication interface on the hot plug module*** to establish a communication link with a running computing device, Olarig does not anticipate claims 1, 7, 8 and 9. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejections be reversed.

The examiner rejected **claims 1-5, 7-10, 28-29, 35 and 37** under 35 USC 102(e) as being anticipated by Bealkowski et al. (US Patent 6,282,596).

Appellants submit that each of **claims 1 and 8**, requires ***enabling a communication interface on the hot plug module to establish a communication link with a running computing device***. In the Examiner's Answer, FIGS. 1-3 are cited to support the Examiner's contention that the processor cards 11, 20, and 30 are hot pluggable to the data processing system 10 via the CPU connector 14. Appellants submit that the processor cards 11a-11d are supplied a clock signal, regulated power supply and bus signal through the associated CPU connector 14a-14d (see column 2, lines 28-32). It is thus clear that the processor cards 11a-11d do not have a communication interface but instead that the CPU connectors 14a-14d act as the interface to the respective processor card to facilitate the supply of the clock signal, the power supply, and the bus signal.

Further, in the newly cited column 6, lines 35-39, Bealkowski ***explicitly*** teaches using FET switches 80, 82, 86 to control the signaling between the processor cards

11a-11d and the computer system. Such FET switches 80, 82, 86 are sufficient to provide the isolation described by Bealkowski. As a result, there is no reason to believe that the interfaces of the processor cards 11a-11d have the capability of being enabled ***with a communication interface on the hot plug module to establish a communication link with a running computing device***.

The Examiner's Answer further states, "the processors cards 11a-11d communicate on the bus 18 and therefore must necessarily have input/output capabilities in order for that communication to occur (i.e. each of the processor cards 11a-11d must have communication interface to connect to CPU connectors 14a-d)". Appellants submit that CPU connector appears to connect the processor cards with the system bus in order to supply power but not to establish communication. Therefore, Appellants have been unable to locate where Bealkowski teaches ***enabling a communication interface on the hot plug module*** to establish a ***communication link*** with a running computing device.

Also, the Examiner's Answer (based on column 3, lines 32-41 of Bealkowski) states, "Bealkowski teaches supplying power along with a clock signal to processor card 11a-11d once a processor card is coupled to the system bus 18". Bealkowski discloses supplying power supply to the processor subsystem when it is added to the system and initialization are performed on the processor within the processor subsystem through a controller which transmits initialization data to the processor ***independent of the processor bus***. Appellants submit that Bealkowski has disclosed that the controller is

needed to transmit initialization data to the processor ***independent of the processor bus***. Appellants thus submit that the Examiner's statement, "Bealkowski teaches supplying power along with a clock signal to processor card 11a-11d once a processor card is coupled to the system bus 18" appears to be ambiguous. Additionally, Appellants have been unable to locate where Bealkowski teaches ***enabling a communication interface on the hot plug module*** to establish a ***communication link*** with a running computing device.

Thus, Bealkowski does not teach ***enabling a communication interface on a hot plug module*** as required by Appellants' claims 1 and 8. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejections be reversed.

Appellants submit that each of **claims 2-4** depends from claim 1. Accordingly, each of claims 2-4 is allowable for at least the reasons stated above in regard to claim 1. Furthermore, each of claims 2-4 requires ***both a communication interface on the hot plug module*** and ***a communication interface of a running computer system***.

The Examiner's Answer states, "the processor card 11a-11d must necessarily have its own communication interfaces in order to transfer data to/and from ***CPU connector 14a-d***. The claim language states "enabling a communication interface of the running computing device that is associated with the hot plug module". The Examiner appears to equate ***CPU connector 14*** of Bealkowski with ***communication interface on a hot plug module*** of the Applicants. Appellants submit that a person

skilled in the art would not treat a CPU connector 14 as being similar to the ***communication interface of the hot plug module*** and running computing device as required by the Applicant's claims 2-4.

Thus, Bealkowski does not teach each and every limitation of the Applicant's claims 2-4, Bealkowski does not anticipate claims 2-4. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejection be reversed.

Claim 5 depends from claim 1. Accordingly, claim 5 is allowable for at least the reasons stated above in regard to claim 1. Appellants submit that the above submissions are sufficient to overcome the present rejection of claim 5 under Bealkowski. Appellants respectfully request that the rejection of claim 5 be reversed.

Claim 7 depends from claim 1. Accordingly, claim 7 is allowable for at least the reasons stated above in regard to claim 1. Furthermore, claim 7 requires adding the identified memory of the hot plug module to a ***memory pool to increase the memory pool***. The Examiner's Answer states that Bealkowski, in column 9, lines 42-45, teaches adding memory from a hot plug module to a memory pool. Appellants submit that Bealkowski, in column 9, lines 42-45, only teaches that in removing the processor from operation, the work load is quiesced from the processor, the caches of the processor are flushed and the processor is set to idle.

Appellants submit that Bealkowski does not appear to teach, "adding the identified memory of the hot plug module to a ***memory pool to increase the memory pool***". The Appellants do not believe that "flushing of caches of the processor upon

removal of the processor cards 11a-d" may be equated with "adding the identified memory of the hot plug module to a ***memory pool to increase the memory pool***" as required by Applicant's claim 7. Even if it is presumed that memory is added to hot plug module to increase memory pool, Bealkowski still does not teach any thing about ***identification*** of the hot plug module before adding it to the memory pool. Further, Appellants submit that the arguments stated above in regard to claim 1 are applicable to the patentability of claim 7. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejection be reversed.

Claims 9 and 10 depend from claim 8. Accordingly, claims 9 and 10 are allowable for at least the reasons stated above in regard to claim 8. Furthermore, the arguments stated above for claims 2-4 in regard to requiring both a communication interface of a hot plug module and a communication interface of a running computer system are applicable to the patentability of claims 9 and 10. Appellants respectfully request the rejection of claims 9 and 10 be reversed.

Claim 28 requires a midplane having a hot plug interface and a hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device. The Examiner's Answer states, "since Bealkowski teaches enabling a communication interface on the hot plug module to establish communication link with the running computing device, Beolkowski similarly teaches the limitation, a midplane having a hot plug module to update the state of the

hot plug interface of the midplane to indicate when the resources are ready to join the computing device".

Appellants submit that Bealkowski merely indicates that a service processor and/or a hot plug control of the computer system side of the connector manage FET switches that isolate a processor card during addition and removal. There appears to be no teaching of the processor card updating a hot plug interface on the computer system side of the connector.

Therefore, the Examiner's presumption that by selectively enabling the processor cards 11a-d, the system must have knowledge of when the resources are ready to join appears to be incorrect. Further, Appellants have been unable to locate where Bealkowski teaches a midplane having a hot plug interface and a hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device.

Thus, Bealkowski does not teach each and every limitation of claim 28, Bealkowski does not anticipate Appellants' claim 28. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejection be reversed.

Claim 29 depends from claim 28. Accordingly, claim 29 is allowable for at least the reasons stated above in regard to claim 28. Furthermore, claim 29 requires hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane.

In the newly cited column 8, lines 1-5, Bealkowski discloses that block 108 depicts sending a CFG signal to detect the presence of the particular processor subsystem. However, Appellants have been unable to locate where Bealkowski discloses hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane. Appellants submit that a person skilled in the art would not consider a CFG signal similar to the Appellant's hot plug interrupt generated in response to a change in the signal indicative of whether the coupler of the of the hot plug module has been coupled to the coupler of the midplane.

Thus, Bealkowski does not teach each and every limitation of claim 29, Bealkowski does not anticipate Appellants' claim 29. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejection be reversed.

Claim 35 depends from claim 1. Accordingly, claim 35 is allowable for at least the reasons stated above in regard to claim 1. Furthermore, claim 35 requires transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system.

In newly cited column 4, lines 38-46, Bealkowski discloses that processor 30a-30d and memory element 32 is coupled to a PCI bus 37 of data processing system 10 through a PCI Host Bridge 34. PCI Host Bridge 34 provides a low latency path through which processors may directly access PCI devices mapped anywhere within bus memory and or I/O address space. However, it appears that the PCI Host Bridge is not

provided with the processors 30a-30d. Appellants thus submit that a person skilled in the art would not treat PCI Host Bridge as being similar to the communication interface on the hot plug module and the communication interface of the running computer system.

Thus, Bealkowski does not teach each and every limitation of claim 35, Bealkowski does not anticipate Appellants' claim 35. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejection be reversed.

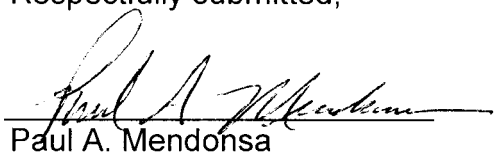
Claim 37 depends from claim 8. Accordingly, claim 37 is allowable for at least the reasons stated above in regard to claim 8. Furthermore, claim 37 requires transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system.

The Examiner's Answer, based on a new citation "PCI Local Bus Specification, Revision 2.2, December 18, 1998, states, "as per PCI specification the data traveling to and from processor card 1a-d must inherently be in the form of packets". Appellants submit that the communicate interface is required, on the hot plug module and with the running computing system, to transfer packets between the communication interface on the hot plug module and the communication interface of the running computing system. Appellants submit that even if it is presumed that data is transferred in the form of the packets, still Bealkowski does not teaches that communication interface is provided with the hot plug module. Appellants therefore respectfully disagree with the position of the Examiner and request that the rejection be reversed.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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